UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,426	03/09/2004	Brian Robert Prasky	POU920030068US1	1895

7590 04/24/2006

Richard M. Goldman
Suite 208
371 Elan Village Lane
San Jose, CA 95134

EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,426	PRASKY ET AL.	
	Examiner	Art Unit	
	Dillon J. Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, all filed 9 March 2004.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. The disclosure is objected to because of the following informalities:

   a. Paragraph 16, line 7: "interaction" should read "iteration"

   b. Paragraph 19, line 4: "transfer" should read "target"

5. Appropriate correction is required.

Claim Objections

6. Claims are objected to because of the following informalities:

   c. Claims 4, 27 and 31: "full associative" should read "fully associative"

d. Claims 5, 14, 17, 22, 23, 44, 49 and 50: "comprising" should follow the preamble of the claim. For example: "The method of claim 1 comprising and entry..." for claim 5.

e. Claims 10 and 37: The claim language is confusing and does not constitute a sentence. It appears that "depth in respect to" should be replaced with "for".

f. Claim 11: "supports" should read "support"

g. Claim 24: "comprising" should be deleted from line 2.

h. Claim 28: "to" should be deleted from line 2.

i. Claim 36: "where" should be deleted from line 3.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 28-50 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A "program product" is not considered to be tangible, and is, hence, considered to be non-statutory.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-5, 7-13, 15-32, 34-40 and 42-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Stiles et al. (U.S. Patent No. 6,425,075) hereinafter referred to as Stiles.

12. As per claim 1, Stiles teaches a method of operating a computer having a pipelined processor having a branch target buffer (BTB) (Fig. 2 cache 155) comprising creating a recent entry queue (Fig. 2 cache 152) in parallel with the branch target buffer (BTB).

13. As per claim 2, Stiles teaches the method of claim 1 wherein the recent entry queue comprises a set of branch target buffer (BTB) entries. (Col. 3 lines 28-38)

14. As per claim 3, Stiles teaches the method of claim 2 comprising organizing the recent entry queue as a FIFO queue. (Col. 10 lines 37-40) *The examiner asserts that Stiles' invention removes entries from the L1 BPC in the order in which they were accessed. The first to be accessed are the first to be removed.*

15. As per claim 4, Stiles teaches the method of claim 3 wherein the recent entry queue is full[y] associative for reading. (Col. 3 lines 63-64)

16. As per claim 5, Stiles teaches the method of claim 1 [comprising] comparing an entry to be written into the BTB against the valid entries within the recent entry queue. (Col. 10 lines 41-67) *The examiner asserts that upon writing an entry into the cache, entries must be compared to find the appropriate destination for the new entry.*

17. As per claim 7, Stiles teaches the method of claim 5 wherein when an entry is written into the BTB it is also written into the recent entry queue. *The examiner asserts that the L1 BPC holds only recent branch data and the L2 BPC holds data covering a longer history of branches. Inherently, if branch data is to be retained longer than the L1 BPC can hold it, it must also be written into the L2 BPC.*

18. As per claim 8, Stiles teaches the method of claim 1 comprising searching the BTB for a next predicted branch and evaluating the recent entry queue while the BTB is being indexed. (Col. 9 lines 35-37)

19. As per claim 9, Stiles teaches the method of claim 8 wherein the recent entry queue maintains a depth up to the associativity of the BTB whereby while the BTB is indexed, the recent entry queue positions are input to comparison logic. *The examiner asserts that the L1 BPC maintains a depth of as many entries as possible, as dictated by the LRU replacement algorithm (col. 10 lines 37-40). Further, since the L2 BPC is disclosed as being direct mapped, (col. 16 line 7) it has an associativity of 1. The L1 BPC has been disclosed as having a depth greater than 1.*

20. As per claim 10, Stiles teaches the method of claim 8 comprising searching the recent entry queue [for] a matching branch in parallel to searching BTB output. (Col. 9 lines 35-37)

21. As per claim 11, Stiles teaches the method of claim 10 comprising creating hit detect logic to support the associativity of the BTB. (Col. 16 lines 10-20)

22. As per claim 12, Stiles teaches the method of claim 8 comprising using a subset of the recent entry queue as a subset of the BTB. *The examiner asserts that since an branch data entry can be indexed into both the L1 and L2 BPC, the entries in the L1 BPC constitute a subset of those in the L2.*

23. As per claim 13, Stiles teaches the method of claim 12 comprising fast indexing recently encountered branches. *The examiner asserts that since the L1 BPC holds fewer entries, it inherently can be checked for a pending branch more quickly than the L2 BPC, which stores many more entries.*

24. As per claim 15, Stiles teaches the method of claim 1 comprising searching the recent entry queue to detect looping branches. *The examiner asserts that the L1 BPC is searched to detect <u>any</u> branch entry, including looping branches.*

25. As per claim 16, Stiles teaches the method of claim 15 comprising comparing the branch to determine if it was recently written into the queue. *The examiner asserts that if an entry appears in the L1 BPC, it was recently written.*

26. As per claim 17, Stiles teaches the method of claim 16 [comprising] determining if the branch is backwards branching whereby a looping branch is detected. *The examiner asserts that if the stored target address is of a lower value than the current PC address, the branch is inherently identified as a backwards branch.*

27. As per claim 18, Stiles teaches the method of claim 17 comprising first detecting a looping branch is detected that is not predicted, and thereafter delaying a decode. *The examiner asserts that when any branch is mispredicted (including a looping branch) the pipeline must flush pending operations (col. 16 lines 15-18). In order the flush the pipeline, the subsequent instruction must inherently be delayed to allow the flush to complete.*

28. As per claim 19, Stiles teaches the method of claim 18 comprising delaying decode until a fixed number of cycles. *The decode is inherently delayed by the number of clock cycles it takes to flush the pipeline.*

29. As per claim 20, Stiles teaches the method of claim 19 comprising delaying decode until the BTB predicts a branch. *Inherently, the branch target instruction will not be decoded until it has been predicted to have been taken.*

30. As per claim 21, Stiles teaches the method of claim 1 comprising staging writes to the BTB in the recent entry queue. *The examiner asserts that BTB writes are stored in the L1 BPC (Col. 3 lines 27-38)*

31. As per claim 22, Stiles teaches the method of claim 21 [comprising] delaying a write and placing the write in the recent event queue. *The examiner asserts that a write to the BTB is delayed until the first iteration of the branch has been evaluated for target address and direction. Since the L1 BPC stores this information (col. 3 lines 48-55) it is not possible to place the data in the BPC until it has been calculated.*

32. As per claim 23, Stiles teaches the method of claim 22 [comprising] detecting a predicted branch while its BTB write is temporarily staged in the recent entry queue. (Col. 3 lines 28-38)

33. Claim 24 is directed toward a computer implementing the method of claim 1 and is rejected under the same grounds as stated above.

34. Claim 25 is directed toward a computer implementing the method of claim 2 and is rejected under the same grounds as stated above.

35. Claim 26 is directed toward a computer implementing the method of claim 3 and is rejected under the same grounds as stated above.

36. Claim 27 is directed toward a computer implementing the method of claim 4 and is rejected under the same grounds as stated above.

37. Claims 28-32, 34-40, and 42-50 are directed toward a program product implementing the method of claims 1-5, 7-13, and 15-23, respectively, and are rejected under the same grounds as stated above.

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 6, 14, 33, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles.

40. As per claim 6, Stiles teaches the method of claim 5 but fails to disclose it comprising blocking an entry matching an entry within the recent entry queue from being written into the BTB.

41. Official Notice is taken that arranging the caches in a tiered arrangement (like a typical L1-L2 cache setup) is well known in the art. A tiered arrangement of cache levels allows the system to write an entry into only the L1 cache rather than spending the time and resources to write into both the L1 and L2. Upon eviction from the L1 cache, the entry is written into the L2. The examiner asserts that with this arrangement, any entry (including those that match current entries in the L1) will be blocked from writing to the L2 cache.

42. It would have been obvious to one of ordinary skill in the art at the time of invention to have arranged Stiles' caches in a tiered L1-L2 arrangement for the benefit of conserving system resources on writing an entry to the BTB.

43. As per claim 14, Stiles teaches the method of claim 12 but fails to teach it [comprising] searching the complete recent entry queue to block duplicate BTB writes.

44. Official Notice is taken that updating an existing entry in a cache is well known in the art. Checking for an existing entry eliminates the wasting of memory space for a pending store which matches an entry already in the cache.

45. It would have been obvious to one of ordinary skill in the art at the time of invention to have checked the L1 BPC for an existing entry before writing into a new position for the benefit of not wasting memory space.

46. Claim 33 is directed toward a program product implementing the method of claim 6 and is rejected under the same grounds as stated above.

47. Claim 41 is directed toward a program product implementing the method of claim 14 and is rejected under the same grounds as stated above.

Conclusion

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McDonald (U.S. Publication No. 2004/0139281) discloses a BTB with write queue storing pending entries to the BTB.

Emma et al. (U.S. Patent No. 5,434,985) disclose a processor with update queue storing pending entries for the branch history table.

49. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100